Claims

1. A flash memory array with improved erasure performance comprises of a plurality of sectors of floating gate memory cells, each said sector of floating gate memory cells includes a plurality of groups of floating gate memory cells, each said group of floating gate memory cells includes one or more wordlines of floating gate memory cells, wherein erasure of said flash memory array is carried out by erasing said groups of floating gate memory cells individually.

2. The flash memory array of claim 1, wherein wordlines in each said group of floating gate memory cells connects to a voltage selecting means, said voltage selecting means being controlled by an address decoding means that is common to all wordlines in a group.

3. The flash memory array of claim 2, wherein said voltage selecting means comprises of a first and second NMOS transistor connect in a serial manner, with the source of said first NMOS transistor connected to the drain of said second NMOS transistor to form a common node, the drain of said first transistor connected to a voltage supply line while the source of said second NMOS transistor being connected to ground, the gates of said first and second NMOS transistors being connected to a first and second output terminals of said address decoding means respectively, a wordline connects to said common node whereby a high voltage signal to the gate of said first NMOS transistor and a low voltage signal to the gate of said second NMOS transistor would connects said voltage supply line to said wordline.

4. The flash memory array of claim 3, wherein a low voltage to the gate of said first NMOS transistor and a high voltage to the gate of said second NMOS transistor would isolates said wordline from said voltage supply line.

5. The flash memory array of claim 2, wherein said voltage selecting means comprises of a first and second PMOS transistor connect in a serial manner, with the drain of said first PMOS transistor connected to the source of said second PMOS transistor to form a common node, the source of said first transistor connected to a voltage supply line while the drain of said second PMOS transistor being connected to ground, the gates of said first and second PMOS transistors being connected to a first and second output terminals of said address decoding means respectively, a wordline connects to said common node whereby a low voltage signal to the gate of said first PMOS transistor and a high voltage signal to the gate of said second PMOS transistor would connects said voltage supply line to said wordline.

6. The flash memory array of claim 5, wherein a high voltage to the gate of said first PMOS transistor and a low voltage to the gate of said second PMOS transistor would isolates said wordline from said voltage supply line.

7. A method of erasing a floating gate memory array that includes a plurality of sectors of floating gate memory cells, each said plurality of sectors includes a plurality of wordlines of floating gate memory cells, the method comprising:

- organizing each of said plurality of sectors of floating gate memory cells into groups of wordlines, each group of wordlines having a common address decoding switch that will pass an erasure voltage to said group of wordlines only when a certain address is decoded; and
- isolating each said group of wordlines from said controlling voltage when a certain group of addresses is not decoded.